What is claimed is:

1. A method of reducing power consumption in a semiconductor memory device having a row of memory cells and circuitry for operating the row of memory cells, the method comprising the steps of:

providing an intervention circuit;

instantiating the intervention circuit within the circuitry for operating the row of memory cells, proximal to the row of memory cells;

operating the intervention circuit to retain the row of memory cells in a desired state; and

powering down the circuitry for operating the row of memory cells preceding the intervention circuit.

2. The method of claim 1,wherein the row of memory cells comprises a wordline and the circuitry for operating the row of memory cells comprises driver circuitry.

3. The method of claim 1, wherein the intervention circuit comprises a resistor.

4. The method of claim 1, wherein the intervention circuit comprises a transistor.

5. The method of claim 2, wherein the intervention circuit is instantiated such that the driver circuitry is between the intervention circuit and the wordline.

6. The method of claim 2, wherein the intervention circuit is instantiated between the wordline and driver circuitry.

7. The method of claim 1, wherein the steps of operating the intervention circuit and powering down the control circuitry are performed concurrently.

8. The method of claim 7, wherein the intervention circuit is operated by a signal source that also powers down the control circuitry.

9. The method of claim 1, wherein a nominal delay follows the step of operating the intervention circuit before powering down the control circuitry is performed.

10. The method of claim 9, wherein the intervention circuit is operated by a first signal source, separate from a second signal source that powers down the control circuitry.

11. A semiconductor device comprising:

a row of memory cells;

control circuitry preceding the row of memory cells; and

an intervention circuit, instantiated within the control circuitry proximal to the row of memory cells, adapted to hold the row of memory cells at a desired state while control circuitry preceding the intervention circuit is powered down.

12. The device of claim 11, wherein the row of memory cells comprises a wordline and the control circuitry preceding the row of memory cells comprises driver circuitry.

13. The device of claim 11, wherein the intervention circuit comprises a resistor.

14. The device of claim 11, wherein the intervention circuit comprises a transistor.

15. The device of claim 12, wherein the intervention circuit is instantiated such that the driver circuitry is between the intervention circuit and the wordline.

16. The device of claim 12, wherein the intervention circuit is instantiated between the wordline and driver circuitry.

17. The device of claim 12, wherein the intervention circuit is coupled to a first assertion signal source that is also coupled to the driver circuitry.

18. The device of claim 12, wherein the intervention circuit is coupled to a first assertion signal source, and a second assertion signal source is coupled to the driver circuitry.

19. A wordline circuitry segment in an SRAM device, the circuitry segment comprising:

a first node coupled to a wordline enable signal;

a second node coupled to a wordline signal;

a third node coupled to a sleep mode assertion signal;

a fourth node coupled to a first reference voltage;

a fifth node coupled to a second reference voltage;

a first transistor structure, having a first terminal coupled to the first node, a second terminal coupled to the fourth node, and a third and fourth terminal;

a second transistor structure, having a first terminal coupled to the fourth terminal of the first transistor structure, a second terminal coupled to the fourth node, a third terminal coupled to the third terminal of the first transistor structure, and a fourth terminal coupled to the second node;

a third transistor structure, having a first terminal coupled to the third node, a second terminal coupled to the third terminal of the first transistor structure, and a third terminal coupled to a third reference voltage; and

a fourth transistor structure, having a first terminal coupled to the fifth node, a second terminal coupled to the fourth node, and a third terminal coupled to the second node.

20. The circuitry segment of claim 19, wherein the fifth node is coupled to the third node.

21. A wordline circuitry segment in an SRAM device, the circuitry segment comprising:

a first node coupled to a wordline enable signal;

a second node coupled to a wordline signal;

a third node coupled to a sleep mode assertion signal;

a fourth node coupled to a first reference voltage;

a fifth node coupled to a second reference voltage;

a sixth node coupled to a third reference voltage;

a first transistor structure, having a first terminal coupled to the first node, a second terminal, a third terminal coupled to the fifth node, and a fourth terminal;

a second transistor structure, having a first terminal coupled to the fourth terminal of the first transistor structure, a second terminal coupled to the fourth node, a third terminal coupled to the fifth node, and a fourth terminal coupled to the second node;

a third transistor structure, having a first terminal coupled to the third node, a second terminal coupled to a fourth reference voltage, and a third terminal coupled to the second terminal of the first transistor structure; and

a fourth transistor structure, having a first terminal coupled to the sixth node, a second terminal coupled to the first terminal of the second transistor structure, and a third terminal coupled to the fifth node.

22. The circuitry segment of claim 21, wherein the sixth node is coupled to the third node.